REMARKS

The Office Action dated January 24, 2006 has been received and considered. In this response, claims 1 and 33 have been amended and claims 2-9, 11-14 and 34-40 have been canceled without prejudice or disclaimer. Specifically, independent claim 1 has been amended to recite the additional features of claim 13 (which depends directly from claim 1), and all other claims depending from claim 1 have been canceled. Independent claim 33 has been amended to recite the additional features of claim 36 and intervening claim 35, and all other claims depending from claim 33 have been canceled. Thus, claim 1 presently has the same scope as previously-presented claim 13 and claim 33 presently has the same scope as previously-presented claim 36. Accordingly, these amendments do not necessitate any additional search or consideration on the part of the Office. Reconsideration of the outstanding rejection in the present application therefore is respectfully requested based on the following remarks.

Obviousness Rejection of Claims 1-6, 8-10, 13, 14, 33-36 and 41

At page 2 of the Office Action, claims 1-6, 8-10, 13, 14, 33-36 and 41 are rejected under 35 U.S.C. Section 103(a) as being unpatentable over Easter (U.S. Patent No. 5,563,950) in view of Van Oorschot (U.S. Patent No. 5,850,443).[1] This rejection is respectfully traversed.

Claims 2-6, 8-10, 13, 14, and 34-36 have been canceled without prejudice or disclaimer.

Independent claim 1 has been amended to additionally recite the features of dependent claim 13. Claim 1 presently recites the features of a memory location having an output port, wherein a data value to be stored in said memory location is observable only internally to the monolithic semiconductor device, and at least one silicon die pad having an input coupled to the output port of said memory location to provide temporary access to said memory location. The Office Action asserts the key array 25/fuse array 51 of Easter discloses the claimed memory location feature and that Figure 2 of Easter and the passage of Easter at column 4, lines 50-65

[1] The Office Action actually rejects these claims as anticipated under § 102(e). However, it is noted that an anticipation rejection normally is improper in view of a combination of two or more references. Accordingly, this rejection is treated as an obviousness-type rejection for the purposes of this response.

disclose the claimed silicon die pad feature. For ease of reference, the cited passage of Easter is reproduced in its entirety:

> Single IC chip 63 includes input buffer 15 and output buffer 17 that control I/O with CPU 13 over internal busses 35 and I/O bus 14. An RSA engine 57 is provided as a public key cryptography engine. All of these elements are interconnected by bussing 35. Further, key storage is provided by a combination of a fuse array 51 and a key array 25 that are connected to RSA engine 57 via key transfer busses 37.
> Key storage facilities for RSA engine 57 are provided by a combination of key array 25 and fuse array 51. To recall, public key cryptographic engines (such as RSA engine 57) require the use of a private key and a public key. In accordance with the present invention, the private key is contained within a non-volatile memory comprising fuse array 51, while the public key is loadable into a volatile memory (such as a random access memory, a "RAM") comprising key array 25.

Easter, col. 4, lines 50-65.

It is respectfully submitted that, contrary to the assertions of the Office Action, the above-cited passage of Easter fails to disclose, or even suggest, the claimed silicon die pad feature. As a first issue, neither the cited passage of Easter nor any other passage of Easter discloses or suggests a silicon die pad in any manner, much less a silicon die pad having an input coupled to an output of the key array 25/fuse array 51 (assuming, arguendo, the key array 25/fuse array 51 is equivalent to the claimed memory location feature). As a second issue, neither this cited passage nor any other passage of Easter discloses or suggests that a silicon die pad is used to provide temporary access to the key array 25/fuse array 51. Thus, Easter fails to disclose or suggest the claimed silicon die pad feature. Van Oorschot likewise fails to disclose or suggest the claimed silicon die pad feature, and the Office Action does not assert that Van Oorschot in fact discloses the claimed silicon die pad feature. Thus, the proposed combination of Easter and Van Oorschot fails to disclose or suggest each and every feature recited by claim 1.

Independent claim 41 recites the features of at least one silicon die pad having an input coupled to the output of said memory location to provide temporary access to said memory location. The Office Action rejects claim 41 under the same rationale as the rejection of claim 13 (the subject matter of which claim 1 presently recites). However, as noted above with respect to claim 1, Easter and Van Oorschot fail to disclose or suggest, alone or in combination, the

claimed silicon pad die feature. Thus, the proposed combination of Easter and Van Oorschot fails to disclose or suggest each and every feature recited by claim 41.

Independent claim 33 has been amended to recite the additional features presented by dependent claim 36 and intervening claim 35. Claim 33 therefore presently recites the features of: accessing, by a first encryption engine internal to a monolithic semiconductor device, data from a memory location internal to the monolithic semiconductor device, wherein the memory location is accessible only internal to the monolithic semiconductor device; generating, at the first encryption engine, a first encryption key based on the data from the memory location, wherein the data represents a second encryption key; and providing the first encryption key for storage in the memory location. The Office Action asserts that the key array 25/fuse array 51 of Easter discloses the claimed memory location feature, the RSA engine 57 of Easter discloses the claimed first encryption engine feature, and that Figure 5 of Easter and the passage of Easter at col. 8, lines 18-26 disclose the claimed feature of providing the first encryption key (generated by the first encryption device) for storage in the memory location. For ease of reference, the cited passage of Easter is reproduced in its entirety:

> Keys for DES encryption engine 21 are stored in key array 25. This is a programmable storage area comprising, for example, RAM. Operationally, keys are transferred for use as DES master keys via public key cryptography techniques using RSA engine 57. One technique for such transfer is described in Munck et al., incorporated by reference hereinabove. Advantageously, using the techniques of the present invention, the private key is secured and the disadvantages of prior manual key-loading systems are overcome.

Easter, col. 8, lines 18-26.

Thus, assuming, *arguendo*, that the key array 25/fuse array 51 is equivalent to the claimed memory location feature, the RSA engine 57 is equivalent to the claimed first encryption engine feature, Easter would have to disclose or suggest that an encryption key generated by the RSA engine 57 is stored in the key array 25/fuse array 51 to be consistent with the claimed feature of providing the first encryption key for storage in the memory location. However, contrary to the assertions of the Office Action, Easter fails to disclose or suggest this feature. As will be appreciated, the cited passage of Easter reproduced above fails to disclose or suggest that any encryption keys generated by the RSA engine 57 are stored in the key array 25/fuse array 51.

Rather, this cited passage merely provides that "keys are transferred for use as DES master keys via public key cryptography techniques using RSA engine 57. One technique for such transfer is described in Munck, et al. . . . " *Id.* Turning to Figure 5 of Easter, Easter illustrates that the connection between the key array 25/fuse array 51 as a unidirectional arrow from the key array 25/fuse array 51 to the RSA engine 57, but Easter does not provide any indication that the connection is bidirectional from the RSA engine 57 to the key array 25/fuse array 51. Further, Figure 5 illustrates that the only output of the RSA engine 57 is connected to the buses 35 and 35' and fails to illustrate that the output of the RSA engine 57 is connected to an input of the key array 25/fuse array 51 in any manner. In fact, Figure 5 fails to illustrate any input to the key array 25/fuse array 51. Thus, in view of Figure 5 of Easter and the corresponding disclosure of Easter, one of ordinary skill in the art would not interpret Easter as disclosing or suggesting that an encryption key output by the RSA engine 57 is provided for storage in the key array 25/fuse array 51. Moreover, Van Oorschot fails to disclose this claimed feature. Thus, the proposed combination of Easter and Van Oorschot fails to disclose or suggest each and every feature recited by claim 33.

In view of the foregoing, it is respectfully submitted that the rejection of claims 1, 33 and 41 is improper at this time. Reconsideration and withdrawal of this rejection therefore is respectfully requested.

Obviousness Rejection of Claim 7

At page 7 of the Office Action, claim 7 is rejected under 35 U.S.C. Section 103(a) as being unpatentable over Easter in view of Loh (U.S. Patent Pub. No. 2003/0093661). This rejection is respectfully traversed. Claim 7 has been canceled without prejudice or disclaimer. Withdrawal of this rejection therefore is respectfully requested.

Obviousness Rejections of Claims 11, 12, 17-22, 24-29, 30-32

At page 7 of the Office Action, claims 11, 12, 17-19, 21, 22, 24-29, 30-32 are rejected under 35 U.S.C. Section 103(a) as being unpatentable over Easter in view of Van Oorschot and further in view of Pitts (U.S. Patent Pub. No. 2002/0145931). At page 13 of the Office Action, claim 20 is rejected under 35 U.S.C. Section 103(a) as being unpatentable over Easter in view of

Van Oorschot and further in view of Pitts and further in view of Loh. These rejections are respectfully traversed.

As stated in MPEP Section 2143, to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). Also, as stated in MPEP Section 2143.01, obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); In re Jones, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990). Additionally, as stated in MPEP Section 2141.02, a prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention. *W.L. Gore & Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984).

Claims 11 and 12 have been canceled without prejudice or disclaimer.

Independent claim 17 recites the features of an external data port having an input and an output, a memory location having an output coupled to an input of a first encryption engine, and an isolation portion coupled to the output of said memory location and to the input of said external data port, wherein said isolation portion is modifiable to permanently prevent access of said memory location by the external data port. The Office Action acknowledges that Easter and Van Oorschot fail to disclose the claimed isolation portion feature. The Office Action therefore relies on Pitts as disclosing an isolation fuse element that enforces one time programming of the

memory. *Office Action*, p. 9. The Office Action therefore asserts that it would have been obvious "to include a fuse element in the semiconductor device [of Easter] because [a] semiconductor device with [a] fuse is well known in the art. Therefore it would have been obvious . . . to combine the teachings of Pitts within the system of Easter because it prevents external access to the memory location after data has been successfully stored into secure memory array." *Id.*

In contrast with the assertions of the Office Action, it is respectfully submitted that one of ordinary skill in the art would not be motivated to combine the teachings of Easter and Pitts as proposed. As noted by the Office Action, Pitts discloses a technique for preventing *external* access to a memory array 108 via the *external* data path 118 of the circuit 100 by implementing an AND gate 110 and fuse element 112 in the external data path 118. *See, e.g., Pitts*, FIG. 1. However, Easter does not disclose that the key array 25/fuse array 51 (which would be analogous to the memory 108 of Pitts) is connected to or accessible an *external* data path of the IC chip 63. Further, Easter provides no indication that the connection of the key array 25/fuse array 51 to an *external* data path of the IC chip 63 would be desirable or advantageous in any way. Thus, as Easter fails to disclose an *external* data path that accesses the key array 25/fuse array 118 in which the AND gate 110 and the fuse 112 can be implemented, one of ordinary skill in the art would find no motivation to utilize the AND gate 110 and fuse element 112 taught by Pitts in the circuit of Easter. As there is no motivation to combine the teachings of Easter and Pitts as proposed by the Office Action, the Office Action fails to establish a *prima facie* case of obviousness for claim 17, as well as claims 18-22 and 24-32 at least by virtue of their dependency from claim 17.

Moreover, these dependent claims recite additional novel features. To illustrate, claim 31 recites the additional features of at least one silicon die pad coupled to the output of said memory location to provide temporary external access to said memory location. As explained above with respect to claim 1 and 41, none of the cited references disclose or suggest, individually or in combination, this claim feature.

In view of the foregoing, it is respectfully submitted that the obvious rejections are improper at this time. Reconsideration and withdrawal of these rejections therefore is respectfully requested.

Conclusion

The Applicant respectfully submits that the present application is in condition for allowance, and an early indication of the same is courteously solicited. The Examiner is respectfully requested to contact the undersigned by telephone at the below listed telephone number in order to expedite resolution of any issues and to expedite passage of the present application to issue, if any comments, questions, or suggestions arise in connection with the present application.

The Commissioner is hereby authorized to charge any fees that may be required, or credit any overpayment, to Deposit Account Number 50-1835.

24 March 2006
Date

Respectfully submitted,

Ryan S. Davidson, Reg. No. 51,596
LARSON NEWMAN ABEL POLANSKY & WHITE, L.L.P.
5914 West Courtyard Dr., Suite 200
Austin, Texas 78730
(512) 439-7100 (phone)
(512) 327-5452 (fax)